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(54) Method of programming an electrically alterable read only memory

(57) In order to store a binary number in a memory row, all the cells of the row are written and then erased. The cells are then written individually so as to represent the binary number. In this way drawbacks due to the degradation of the cells are avoided and the service life of the memory is extended to its maximum length.

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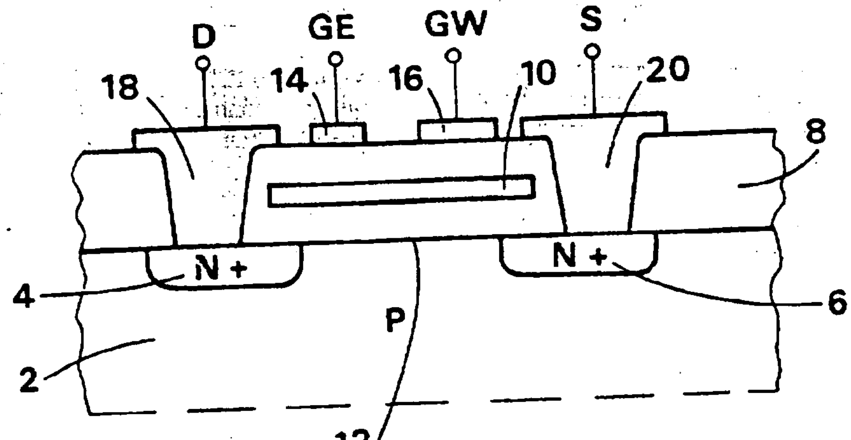
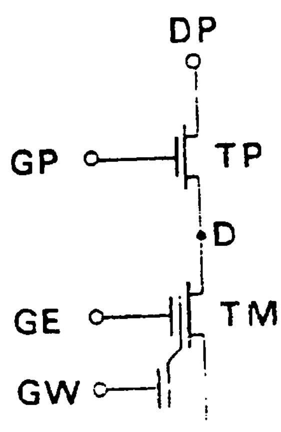


fig.1



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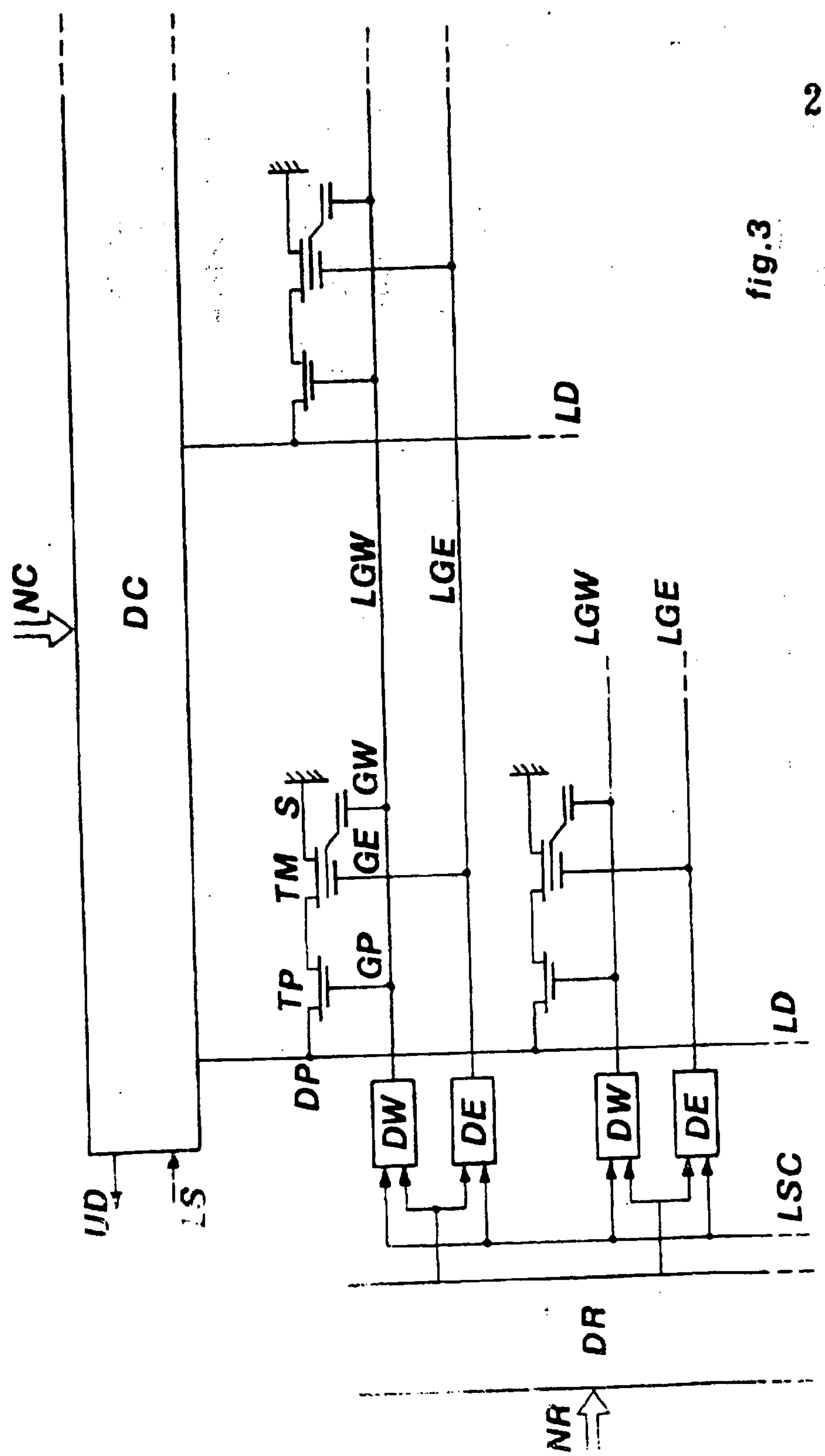

fig.3

SPECIFICATION

Method of programming an electrically alterable read only memory

The present invention relates to an electrically alterable read only memory of the type which may have groups of cells erased and, more particularly, to a programming method, i.e. writing and erasing, for a memory of this type.

Memories of this type are usually known by the abbreviation EAROM (Electrically Alterable Read Only Memory) and use, as the data storage element, a device which functions basically as an insulated gate field effect transistor (IGFET). A device of this type is known and comprises, in addition to the normal source, drain and gate electrodes, a second gate electrode and an electrode which is immersed in the oxide which insulates the gate from the semiconductor substrate and is commonly called "floating gate". By applying suitable voltages between the accessible electrodes of the device it is possible to charge electrons permanently in the floating gate (writing) or to remove electrons from the latter (erasure), as a result of which the memory element may be in two different states, corresponding to two different levels of the conduction threshold of the IGFET transistor, to which it is possible to associate the two levels of a binary datum. Such alterations are possible by means of phenomena of charge transfer across the oxide which surrounds the floating gate. In particular writing takes place by generating high energy electrons in the channel of the IGFET transistor and by applying a high voltage to both the accessible gates. An electrical field which is sufficiently intense to induce the high energy electrons to traverse the oxide until they reach the floating gate in which they are captured, is thus established across the oxide. Erasure is obtained by producing a strong electrical field between the floating gate and one of the two accessible gates. Reading is carried out by examining whether the transistor is conductive or not when a voltage having a value comprised between the two threshold levels defined by the floating gate and its two possible charge states is applied to the accessible gates.

The construction and the operation of a device of this type is described in further detail in the US Patent Specification 3825946.

It has been observed that both the writing time and, in particular, the erasure time, must be increased with an increase in the number of programming cycles. This requirement appears to be due to the fact that conduction across the oxide gradually decreases as result of the capture of the electrons [illegible] oxide itself. This phenomenon obv[illegible] reasonable limits have been fixed [illegible] dification times, limits the service life of the memory, i.e. limits the maximum number of modification cycles to which a cell may be subjected with a positive result.

Designers of this type of memory know how to act on the geometric and physical characteristics of the basic structure of the cell so as to minimise the oxide degradation effects and thus maximise the life of the cell itself, and also know how to increase the modification cycle times to take into account the degradation of the oxide.

The service life of the overall memory structure may be limited, however, not by the maximum of cycles which a single cell may support, but by effects connected with the circuit structure of the matrix of cells of which it is composed.

In particular, a memory in which erasure takes place by cell groups may have cells which are subjected to a large number of erasure cycles in a successive manner before being written for a first time. It has been observed that a cell designed in such a way as to maximise the number of modification cycles, may reach a condition of "over-erasure" which may not be removed with a normal cycle, if it is subjected to a relatively low number of successive erasures. This drawback may be remedied, in accordance with the prior art, only by modifying certain structural characteristics of the cell. However, this requires a movement away from the optimum design criteria, as a result of which the cell has a shorter life than that of the optimum cell. In practice, the reduction of the service life is due to the fact that the initial erasure time, i.e. that of a virgin cell, must be longer than that of an optimum virgin cell, as a result of which as many modification cycles must be given up as are necessary for the erasure time of an optimum cell to reach, in order to compensate the degradation of the oxide, this longer time.

The object of the present invention is to provide a programming method for an EAROM which enables optimum use of cells designed for the maximum number of modification cycles.

According to the present invention there is provided a method of programming an electrically alterable read only semiconductor memory constituted by cells of which comprises a structure functioning as an insulated gate field effect transistor (IGFET) having a conduction threshold designed to have a first stable value higher than a first predetermined level, and a second stable value lower than a second pre[illegible] such a way as to represent [illegible] of a binary number, [illegible] lines and columns [illegible] the storage of data [illegible] cell may be [illegible]ding and writing [illegible] relative lines and

columns and may be made to pass from the written state to the erased state and in which each line may be selected for erasure in such a way that all its cells which are in the written state are brought to the erased state, wherein, in order to store a predetermined sequence of binary numbers in a selected row the following steps are carried out: writing of all the cells of the line which are not already written, erasure of all the cells of the line and writing of those cells of which are to show one predetermined level of the two logic levels which constitute the binary numbers of the sequence to be stored.

The invention will now be described further, by way of example, with reference to the accompanying drawings, in which:

Figure 1 shows, in cross-section and on a very enlarged scale, the active element of a silicon memory of the type having a double layer of polycrystalline silicon;

Figure 2 shows the circuit arrangement of a memory cell incorporating the active element of Fig. 1; and

Figure 3 is a diagram, showing partly by circuit means and partly in blocks, a memory comprising a matrix of cells of the type of Fig. 2 and the relative reading and programming circuits required for implementing the method of the invention.

The construction of Fig. 1 has a substrate 2 of a monocrystalline silicon, doped with P type impurities in which two regions 4 and 6 are formed, these regions being strongly doped with impurities of opposite conductivity (N +) and having the functions of source and drain. The substrate 2 is covered by a layer 8 of silicon dioxide and contains, completely insulated, an electrode 10 called floating gate constituted by polycrystalline silicon doped with impurities of N + type. This electrode extends above the channel 12 defined by the source and drain region 4 and 6. A further two N-type polycrystalline silicon electrodes, indicated by 14 and 16, are disposed on the oxide layer 8 and are each above a portion of the floating gate 10. Two metal electrodes 18 and 20 pass through the oxide layer 8 in order to enable the electrical connection of the source and drain regions 4 and 6 to an external circuit. The gate electrodes 14 and 16 are also connected to an external circuit preferably by means of a doped N-type polycrystalline silicon tracks. The source, drain, cancellation gate and writing gate terminals are indicated by the symbols S, D, GE AND GW respectively.

The above-described structure functions as an N-channel IGFET transistor with an insulated gate, a floating gate and two [illegible] accessible gates and may [illegible] ner known *per se*, in co[illegible] channel enrichment, fi[illegible] normal type, which [illegible] transistor, in order [illegible] alterable read only memory cell The circuit arrangement of the cell is shown in Fig. 2 in which TM represents the storage transistor formed by the construction of Fig. 1 and TP represents the selection transistor. The source electrode of TP is connected to the drain electrode of TM and the terminals of the cell are constituted by the drain DP and the gate GP of TP, as well as by the source S and the writing gate GW and cancellation gate of GE of TM.

The storage transistor TM, as stated in the introduction to the present description, may be in two different electrical states in accordance with the charge present in the floating gate. In the following description it is considered that the cell is written when the conduction threshold of the transistor TM is higher than a first predetermined level and not written, or cancelled, when the threshold of TM is lower than a second predetermined level which is lower than the first.

Operation of the cell of Fig. 2 will now be described. Writing takes place by bringing the drain and the accessible gates to a comparatively high voltage (approx. 25 Volt), in respect of the source electrode S and the substrate 2, which is normally at the same potential as the source S. In these conditions, the transistor TP is conductive, the electrodes acquire high energies in the channel 12 of the transistor TM and, an electrical field which causes the transfer of the high energy electrons into the floating gate is established across the oxide which separates the floating gate 10 from the channel 12. In order to cancel the cell, the cancellation gate GE is maintained at a high voltage (25 Volt) in respect of the source S and the writing gate, i.e. one at least of the terminals GP and DP, is brought to the lowest possible potential. As the result of a capacitive effect, there is formed across the oxide which separates the gate GE from the floating gate 10 an electrical field of sufficient intensity to remove electrons from the floating gate.

As a cell having determined geometrical and morphological characteristics is used and as the levels and the times of application of the operating voltages are fixed, the device TM behaves as an N-channel enrichment field effect transistor having a conduction threshold which is variable between two levels as a function of the charge accumulated in the floating gate. The condition of the cell may be read by applying a voltage lower than the programming voltage to the electrode DP and by applying a voltage to the terminals GP, GE and GW, this voltage being positive in respect of the terminal S and having an amplitude which is not sufficient to modify the charge of the floating gate 10, but sufficient to cause [illegible] transistor TP to conduct in every [illegible] cause the transistor TM to con[illegible] it is in the lower threshold

condition (non-written cell). The absence or presence of current between the source terminal S and the drain terminal DP of the cell, detected by means of a suitable circuit, indicates whether the cell is written or erased respectively. The difference between the two threshold levels is determined at the design stage taking into account, essentially, the variability, due to manufacturing tolerances, of the electrical parameters of the cell, to the degradation of the physical characteristics of the cell during its normal operation and to the sensitivity of the reading circuits.

In order to illustrate the programming method of the invention, reference is now made to Fig. 3, which shows, for reasons of simplicity, only three of a multiplicity of cells forming a memory matrix with the related peripheral circuits. All the cells of the matrix have their source electrode connected to a common, or earth, terminal, and all the cells of a line have their selection gate electrodes GP and writing gate electrodes GW connected together to a row LGW and their erasure gate electrode GE connected to another line LGE. Each of the pairs of lines LGW and LGE of each row is connected to a suitable line decoding circuit, indicated by a block DR, via a line writing drive circuit DW and a line erasure drive circuit DE respectively.

All the cells of a column have their drain electrodes DP connected across a column LD to a decoding and column control circuit, indicated by a block DC. The line and column decoding circuits DR and DC are connected to external circuits (not shown) which generate address signals. The connections for the address signals are provided in parallel by means of groups of terminals, whose number depends on the number of cells of the matrix, and are indicated by NR for line decoding and by NC for column decoding. The column decoding circuit DC has, in addition, a data output terminal UD and an input terminal LS for the read/write command. A similar read/write/erase input terminal LSC is provided for all the line drive circuits DW and DE.

In operation, one cell of the matrix is selected for reading or writing when signals identifying the line and the column at whose intersection the cell is located are present at the inputs NR and NC of the decoding circuits DR and DC. If there is a reading command at the inputs LS and LSC, the lines LGW and LGE and the column LD selected are brought to the predetermined reading voltage and a signal of a high or low level according to the state of the selected cell becomes available at the data output terminal UD. If the writing com[illegible] present at the terminals LS and LSC [illegible] d columns selected receive [illegible] es and the conduction [illegible] selected cell is increased beyond [illegible] minimum written cell level.

Erasure takes place by selecting the line to be erased by means of the application of the corresponding address to the input NR of the line decoder DR and the application of an erasure command to the inputs LSC. In response to this command, the line LGE is brought to the predetermined erasure voltage and the other line LGW is brought to the earth potential.

It is then desired to store a bindary number in a predetermined line of the memory, considering a written cell to contain a "1" and a non-written cell to contain a "0". In accordance with the invention, the cells of the selected line are subjected individually, and preferably in succession, to the writing conditions, as a result of which the non-written cells of the line are written and those which are already written remain written. Since, in general, subjecting a cell which is already written to writing, causes an unnecessary degradation of the cell itself, it is also possible to limit writing to the non-written cells alone. All the cells of the line are then simultaneously erased, as provided for by the circuit connections of the matrix. Finally only the cells of the line designed to show "1" are written.

With the above programming method of the invention as described above, all the cells of each line subjected to modification undergo the same number of erasure cycles from a written cell condition and, therefore, none of them are able to be "over-erased". Consequently, the structure of the cell may be achieved by taking into account solely the design criteria which maximise the number of modification cycles and therefore the service life of the memory is the maximum possible.

CLAIMS (6 Aug 1980)

1. A method of programming an electrically alterable read only semiconductor memory constituted by cells each of which comprises a structure functioning as an insulated gate field effect transistor (IGFET) having a conduction threshold designed to have a first stable value higher than a first predetermined level, and a second stable value lower than a second predetermined level in such a way as to represent the two possible states of a binary number, and connected together by lines and columns so as to form a matrix for the storage of data in binary form, in which each cell may be individually addressed for reading and writing by means of selection of the relative lines and columns and may be made to pass from the written state to the erased [illegible] ine may be [illegible] ll its selec[illegible] ought cells [illegible] [illegible] sure of all

the cells of the line and writing of those cells of the line which are to show one predetermined level of the two logic levels which constitute the bindary numbers of the sequence to be stored.

2. A method of programming an electrically alterable read only memory substantially as hereinbefore described with reference to the accompanying drawings.

CLAIMS (17 Nov. 1980)

1. A method of programming an electrically alterable semiconductor read only memory constituted by cells of each of which comprises a structure functioning as an insulated gate field effect transistor (IGFET) having a conduction threshold designed to have a first stable value higher than a first predetermined level, and a second stable value lower than a second predetermined level in such a way as to represent the two possible states of a binary digit, and connected together by row lines and column lines so as to form a matrix for the storage of data in binary form, in which each cell may be individually addressed for reading and writing by means of selection of the relative row and column lines and may be made to pass from the written state to the erased state and in which each row may be selected for erasure in such a way that all its cells which are in the written state are brought to the erased state, wherein, in order to store a predetermined sequence of binary digits in a selected row, the following steps are carried out: writing of all the cells of the row which are not already written, erasure of all the cells of the row and writing of those cells of the row which are to show one predetermined level of the two logic levels which constitute the binary digits of the sequence to be stored.

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